Abstract of the Disclosure

Disclosed is a bit line precharge signal generator for a memory device, which reduces a resistance component of a signal line by shortening the length of a signal line transferring bit line signals, and reduces an RC time delay. Control signal generator generates a first control signal. A plurality of bit line precharge signal drivers are controlled by first control signal from control signal generator. Each of the bit line precharge signal drivers applies a second signal to the bit line sense amplifier array which is adjacent to bit line precharge signal driver. By using bit line precharge signal generator, a necessary operation is performed within a short time, and unneccessary signal lines are reduced. As a result, a total layout area is reduced.